Revision History:

Rev 01 (08/12/16)

1) Initial release

Rev 02 (03/23/17)

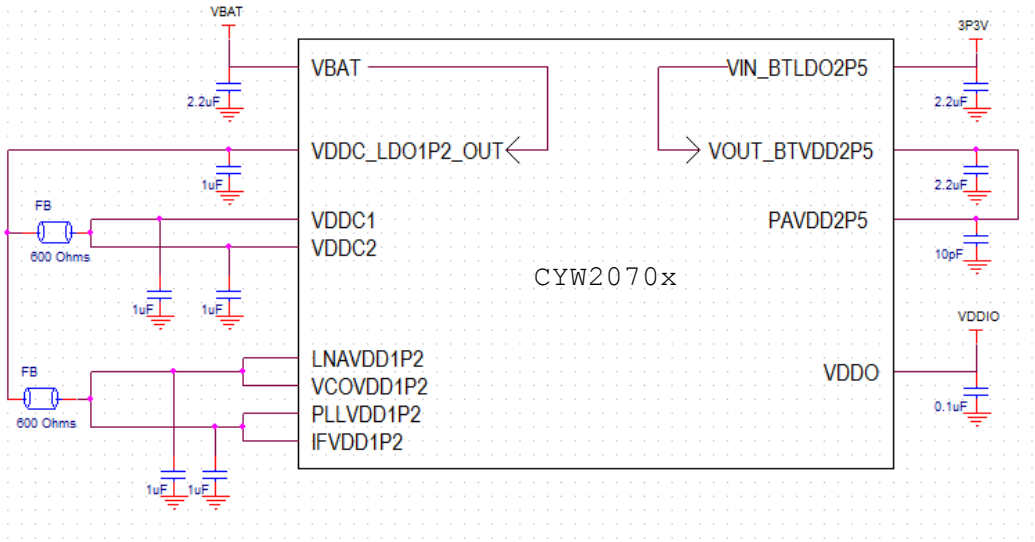
1) Changed J27 to a 10pin debugger
2) Route I2C pins to J21.1 and J21.2
3) Route Pin C8 (I2S_WS/PCM_SYNC/P0/P34) to J23.6

Rev 03 (04/21/17)

1) Removed R74, added J30 instead
2) Removed J6 and J7
3) Connect BT_GPIO_6/P11/P26 to J23.5
4) Connect BT_GPIO_7/P30 to J23.4
5) Connect BT_GPIO_5/P15 to J24.1

Rev 04 (05/16/17)

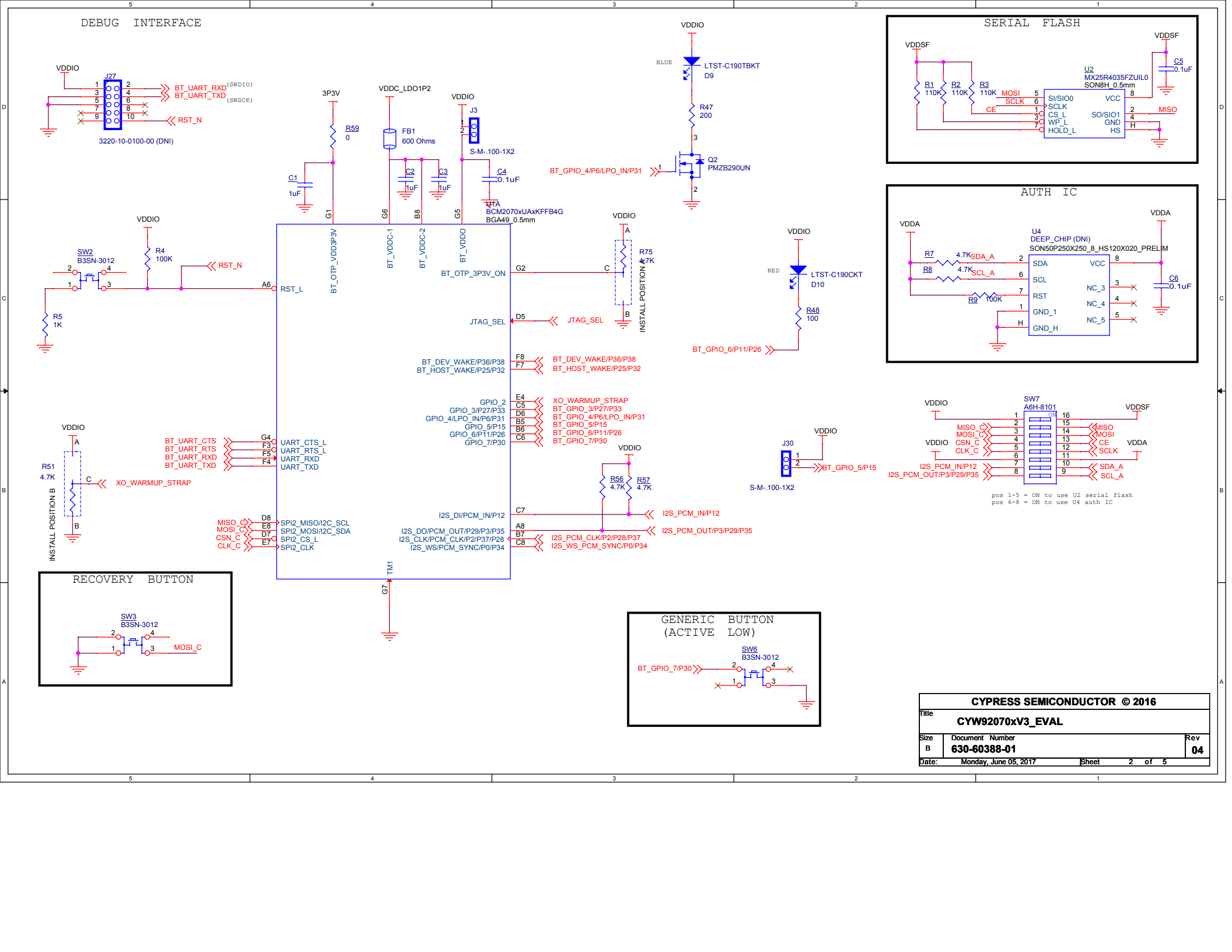
1) Changed R7, R8, R56 and R57 to 4.7K
2) Changed R68 and R69 from DNI to Populate

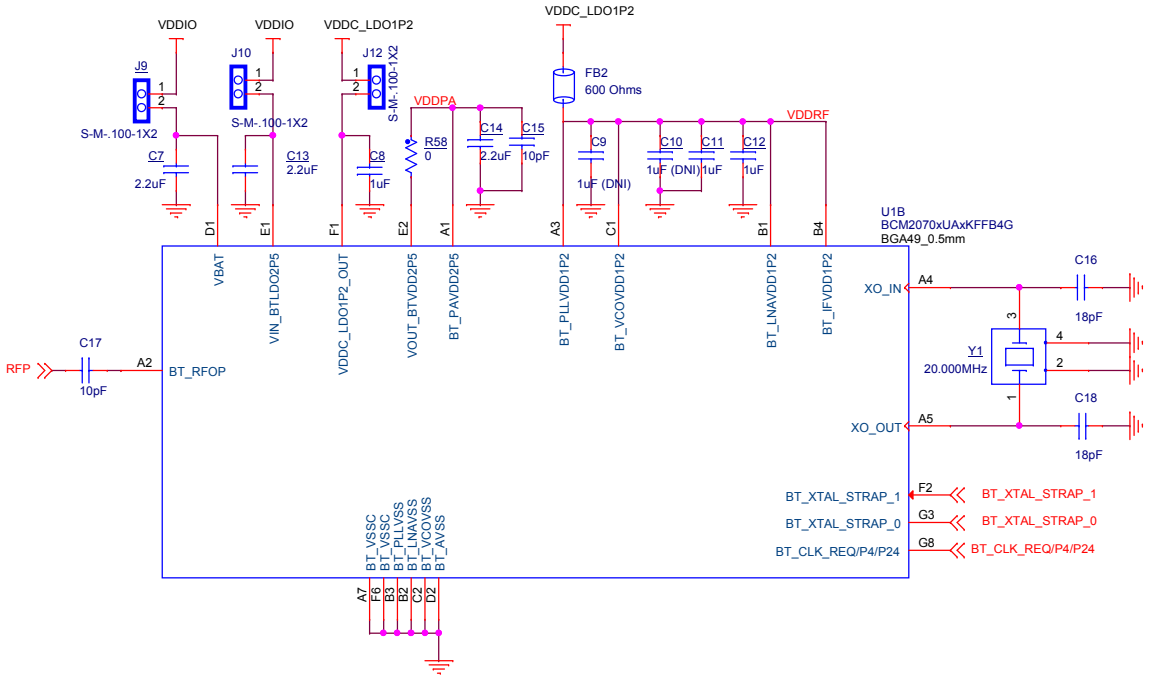


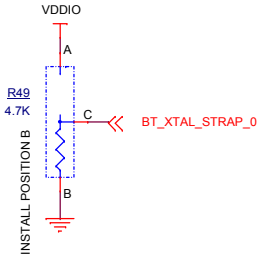
PAGE1: COVER PAGE
PAGE2: BASEBAND & MEMORY
PAGE3: RADIO
PAGE4: POWER & IO
PAGE5: UART

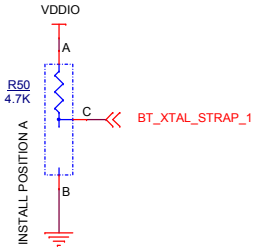
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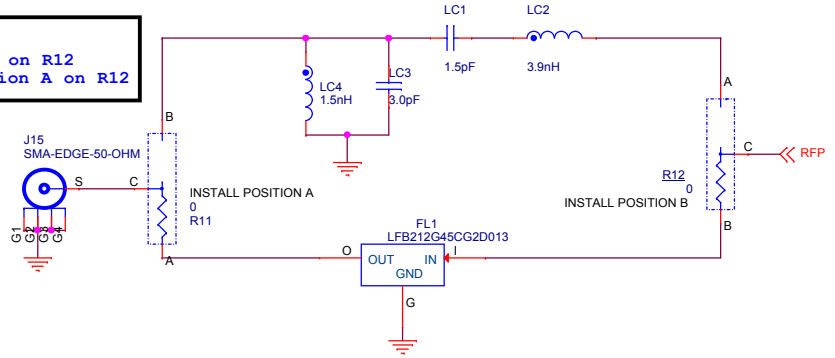

DEBUG INTERFACE
VDDIO
J27
BT_UART_RXD (SWDIO)
BT_UART_TXD (SWDCK)
RST_N
3220-10-0100-00 (DNI)
3P3V
R59
0
C1
1uF
VDDC_LDO1P2
FB1
600 Ohms
C2
1uF
C3
1uF
VDDIO
J3
S-M-.100-1X2
C4
0.1uF
U1A
BCM2070xUAxKFFB4G
BGA49_0.5mm
G1
G6
B8
G5
BT_OTP_VDD3P3V
BT_VDDC-1
BT_VDDC-2
BT_VDDO
VDDIO
SW2
B3SN-3012
R4
100K
RST_N
R5
1K
A6
RST_L
BT_OTP_3P3V_ON
G2
VDDIO
R75
4.7K
INSTALL POSITION A
JTAG_SEL
D5
JTAG_SEL
BT_DEV_WAKE/P36/P38
BT_HOST_WAKE/P25/P32
F8
F7
BT_DEV_WAKE/P36/P38
BT_HOST_WAKE/P25/P32
GPIO_2
GPIO_3/P27/P33
GPIO_4/LPO_IN/P6/P31
GPIO_5/P15
GPIO_6/P11/P26
GPIO_7/P30
E4
C5
D6
B5
B6
C6
XO_WARMUP_STRAP
BT_GPIO_3/P27/P33
BT_GPIO_4/P6/LPO_IN/P31
BT_GPIO_5/P15
BT_GPIO_6/P11/P26
BT_GPIO_7/P30
VDDIO
R51
4.7K
INSTALL POSITION B
XO_WARMUP_STRAP
BT_UART_CTS
BT_UART_RTS
BT_UART_RXD
BT_UART_TXD
G4
F3
F5
F4
UART_CTS_L
UART_RTS_L
UART_RXD
UART_TXD
MISO_C
MOSI_C
CSN_C
CLK_C
D8
E8
D7
E7
SPI2_MISO/I2C_SCL
SPI2_MOSI/I2C_SDA
SPI2_CS_L
SPI2_CLK
I2S_DI/PCM_IN/P12
I2S_DO/PCM_OUT/P29/P3/P35
I2S_CLK/PCM_CLK/P2/P37/P28
I2S_WS/PCM_SYNC/P0/P34
C7
A8
B7
C8
VDDIO
R56
4.7K
R57
4.7K
I2S_PCM_IN/P12
I2S_PCM_OUT/P3/P29/P35
I2S_PCM_CLK/P2/P28/P37
I2S_WS_PCM_SYNC/P0/P34
G7
TM1
VDDIO
J30
BT_GPIO_5/P15
S-M-.100-1X2
VDDIO
BLUE
LTST-C190TBKT
D9
R47
200
Q2
PMZB290UN
BT_GPIO_4/P6/LPO_IN/P31
VDDIO
RED
LTST-C190CKT
D10
R48
100
BT_GPIO_6/P11/P26
SERIAL FLASH
VDDSF
R1
110K
R2
110K
R3
110K
MOSI
SCLK
CE
U2
MX25R4035FZUIL0
SON8H_0.5mm
SI/SIO0
SCLK
CS_L
WP_L
HOLD_L
VCC
SO/SIO1
GND
HS
C5
0.1uF
MISO
AUTH IC
VDDA
U4
DEEP_CHIP (DNI)
SON50P250X250_8_HS120X020_PRELIM
R7
4.7K
SDA_A
R8
4.7K
SCL_A
R9
100K
SDA
SCL
RST
GND_1
GND_H
VCC
NC_3
NC_4
NC_5
C6
0.1uF
SW7
A6H-8101
VDDIO
VDDSF
VDDA
MISO_C
MOSI_C
CSN_C
CLK_C
I2S_PCM_IN/P12
I2S_PCM_OUT/P3/P29/P35
MISO
MOSI
CE
SCLK
SDA_A
SCL_A
pos 1-5 = ON to use U2 serial flash
pos 6-8 = ON to use U4 auth IC
RECOVERY BUTTON
SW3
B3SN-3012
MOSI_C
GENERIC BUTTON
(ACTIVE LOW)
SW6
B3SN-3012
BT_GPIO_7/P30
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Band Pass Filter Options:
Chip BPF: Install Position A on R11 and Install Position B on R12
4 Element BPF: Install Position B on R11 and Install Position A on R12

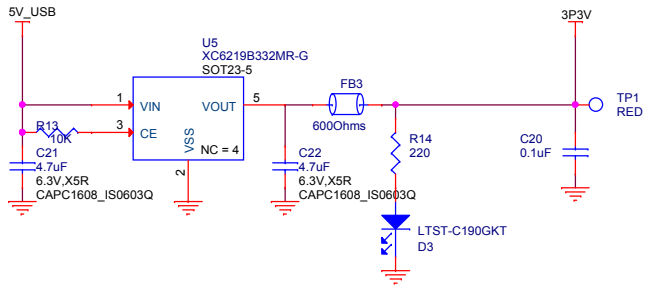


XTAL_STRAP[1:0]	STRAPPING OPTIONS
00	40MHz
01	24MHz
10	20MHz
11	Read from serial flash or EEPROM

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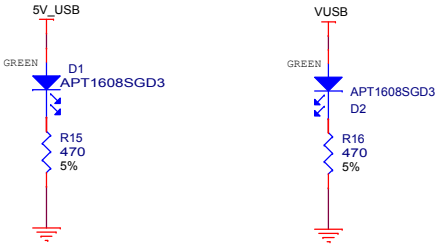
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3.3V 240mA LDO regulator



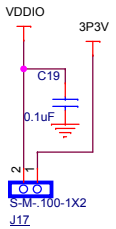
D3: Green, Inducating that 3P3V is on

LED INDICATORS

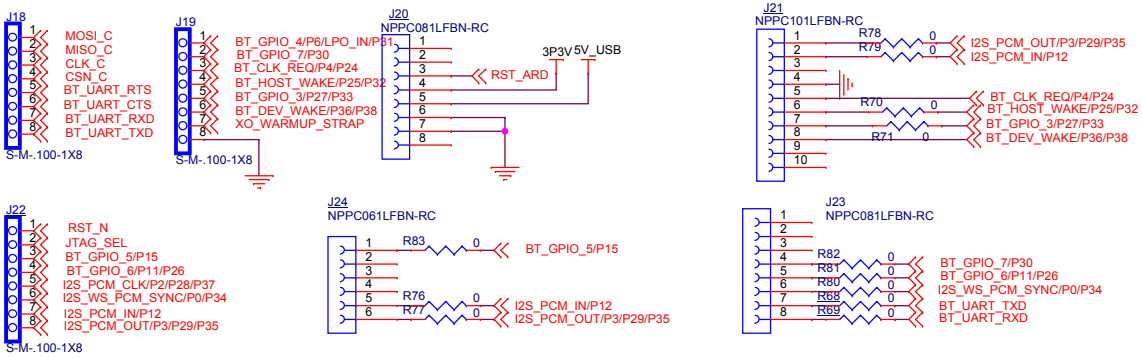


D1: Green, Indicating that Power switch SW4 is switched on.
D2: Green, Indicating that USB cable is plugged in.

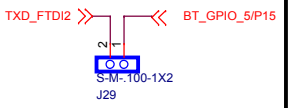
3.3V Jumper



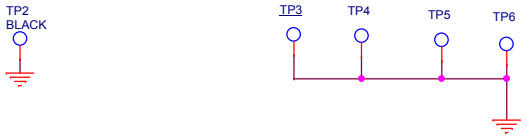
TEST HEADERS



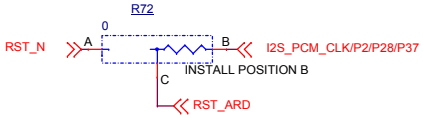
Debug GPIO



GND Test Points

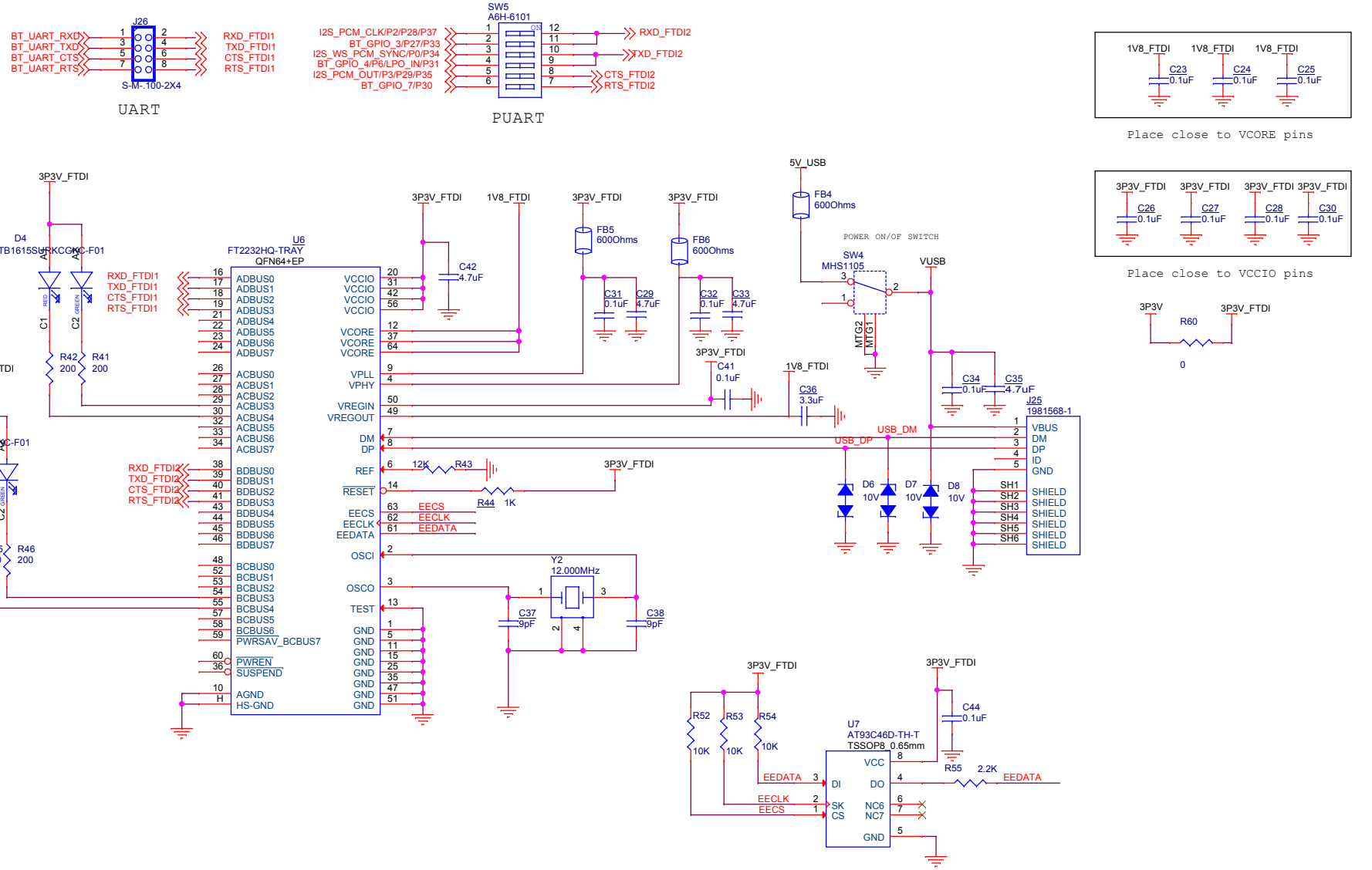


ZJ1 SNT-100-BK-G
ZJ2 SNT-100-BK-G
ZJ3 SNT-100-BK-G
ZJ4 SNT-100-BK-G
ZJ5 SNT-100-BK-G
ZJ6 SNT-100-BK-G
ZJ7 SNT-100-BK-G
ZJ8 SNT-100-BK-G
ZJ9 SNT-100-BK-G



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